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Modulator or Demodulator in Integrated Technology

The invention relates to an integrable active modulator or demodulator with single-ended input and single-ended output.

In the carrier frequency technology as well as in other areas of electrical communication engineering, at present active or passive modulators are used, which use at least one transformer. Such types of circuits are not quite suitable, because the inductances and the transformers can be realized only through the roundabout route of using gyrators and similar, and that too at a great expense. Known are circuits with integrated elements in part, in which the additional transformers with concentrated structures are connected. The hitherto known circuits, which contain only resistors, condensers and semiconductor components like diodes and transistors, have the disadvantage that they require to some extent very high expense, and that, apart from that, the input signal must be balanced.

The underlying problem of the invention lies in providing a modulator or a demodulator of the kind mentioned at the outset, which enables an integrated embodiment with relatively little elaborate circuitry and can therefore be employed as a substitute for ring modulators, especially in frequency converting digital filters.

This problem is solved according to the invention in that the modulator consists of an input stage with outputs, which deliver two separate output signals with the same amplitude, and each of these outputs is connected through a switching four-pole network to an output stage, which combines the output signals of the two switching four-pole networks. The switching four-pole networks are actuated alternately in cyclic timing with a carrier frequency oscillation. The phase of one of the two output signals of the input stage is thereby shifted by 180° either in the input stage or after passing the corresponding switching four-pole network in the output stage.

In the case of the phase rotation in the input stage, it is advantageous to design the input stage as a phase reversal stage, whose output signal amplitudes are the same and in antiphase. In the case of phase rotation in the output stage, the output stage is preferably designed as a differential amplifier and the phase of one of the output signals of the input stage appears with a shift of 180° at the output of the differential amplifier.

Since it is difficult, due to the response times of the circuit elements, to open one switching four-pole network at the same time the other switching four-pole network is closed and vice versa, it is more suitable to regulate the circuit elements in both the switching four-pole networks by two square pulse sequences, derived from the carrier frequency, that are shifted by 180°, whose ratio of the pulse width to the interpulse period is less than 1. In that case it is ensured that in each case only one switching four-pole network is conducting for the output signal of the input stage. For the ratio of the pulse width to the interpulse period of 1/2, there is the additional advantage that the third harmonic of the switching frequency is not present in the generated pole reversal function, as can be determined from the Fourier analysis. It is also

advantageous, if the field effect transistors are used in both the switching four-pole networks, because the offset voltage in the case of field effect transistors is vanishingly small compared to the offset voltage of the commonly used transistors.

By designing the modulator in the aforementioned manner, it can be achieved that only resistors and semiconductor elements like transistors and diodes are required in the circuit of the modulator. A design of the modulator in integrated form is therefore especially easy to realize. An especially preferred area of application of such a modulator is therefore the use in integrated form in frequency converting digital filters.

A few forms of the embodiments of the modulators according to the invention are explained further on the basis of the drawings. Shown are

Fig. 1 a modulator with outputs of the input stage in mutual antiphase,

Fig. 2 another modulator with outputs of the input stage in mutual antiphase,

Fig. 3 a modulator with inputs of the output stage in mutual antiphase,

Fig. 4 another preferred exemplary embodiment of a modulator with outputs of the input stage in mutual antiphase

Fig. 5 evolution in time of the square pulse sequences for regulation of the switching four-pole network of the modulator according to Fig. 1 to Fig. 4.

The modulator according to Fig. 1 contains an input stage I with the input E, transistor T_0, the base voltage divider with the resistors $R1_0$ and $R2_0$, the load resistors $R3_0$ and $R4_0$ and the output terminals A1 and A2 in antiphase, which are connected with the input terminals E1 and E2 of the switching four-pole network SV1 and SV2. The output terminals A3 and A4 for the switching four-pole network are connected in parallel. The modulator represents a counter-cyclic timing modulator, in which both the switching four-pole networks are alternately cut off or connected with one rhythmic timing S1 or S2 in the form of a square pulse sequence derived from the carrier oscillation. At the common output A of both the switching four-poles, side bands with the frequency of the carrier oscillation, which represent the input signal with simultaneous suppression of the carrier wave, are generated in the familiar manner.

The other exemplary embodiments according to Figures 2 to 4 are also balanced modulators. The modulator according to Fig. 2 contains again an input stage I with two amplifiers V1 and V2, whose output terminals A1 and A2 in antiphase are connected to the input terminals E1 and E2 of the two switching four-poles SV1 and SV2. The output terminals A3 and A4 of both the four-pole networks are connected to the input terminals of one of the summers with output A representing the output stage. The switching four-poles SV1 and SV2 contain two field effect transistors FET 1 and FET 2. Their electrodes are shown with the denotations S = source or cathode, D = drain or anode and G = gate or grid customarily used for field effect transistors. The cyclic timings S1 and S2 are fed to the grids G of the field effect transistors through the voltage dividers consisting of the series circuit with a diode D1 or D2 with a resistor R3 or R4. The output terminals A1 and A2 of the input stage I are connected through the resistors R1 and R2, serving among other things as decouplers, directly to the output terminals A3 and A4. The field effect transistors FET 1 and FET 2 are

connected at their respective diodes D at the common connection points of the resistor R1 or R2 with the output terminal A3 or A4, and form, taking their cathodes K at the earth potential into consideration, a regulable short-circuit for the outputs of the switching four-pole networks. In the latter case, it is absolutely necessary that the output stage II is a summing stage, because otherwise the output signal of the entire modulator would be short-circuited.

The modulator according to Fig. 3 contains, as the input stage I, two input amplifiers V1 and V2', of which, in contrast to the amplifier V2 in Fig. 2, the amplifier V2' does not have any phase rotation between input and the output. The switching four-poles SV1 and SV2 have in principle the same design as the switching four-poles according to Fig. 2. They differ from it only in that the normally used transistors T1 and T2 are used in place of the field effect transistors FET 1 and FET 2 and the diodes D1 and D2 in the control circuit are replaced by the resistors R5 and R6. The output stage II is a differential amplifier in this case, which causes the phase reversal in one of the two transmission routes necessary for the function of the balanced modulator.

Fig. 4 shows an especially advantageous exemplary embodiment for a balanced modulator according to the invention. Its input stage I is identical with the input stage I of the modulator according to Fig. 2. While in the exemplary embodiment according

to Fig. 2, the anode-cathode paths of the field effect transistors FET 1 and FET 2 of the switching four-poles SV1 and SV2 are connected in parallel to the outputs of the switching four-poles in the sense of the regulable short-circuits, the anode-cathode paths of the field effect transistors FET1 and FET2 are connected in series with the resistor R1 or R2 between the input terminal E1 or E2 and the output terminal A3 or A4 in the sense of a controllable break in the connection. In this case, cyclic timing S1 or S2 can be fed directly to the grid G of the field effect transistors, that is, the voltage dividers provided in the exemplary embodiment according to Fig. 2 are not needed. The output stage II is here an operation amplifier V3, whose inverting input is connected parallel to the output terminals A3 and A4. The operation amplifier V3 can be dispensed with, if the correct switching behavior of the field effect transistors FET 1 and FET 2 is ensured by means of the corresponding input circuit.

For the sake of completeness, the curves of the cyclic times S1 and S2 at the control inputs of the switching four-poles SV1 and SV2 against time t are shown in Fig. 5. The switching four-poles SV1 and SV2 are conducting for the input signal in the case of "0," while they are blocked in the case of "Z." Since it is hardly possible to achieve with semiconductor components that one switching four-pole opens just at the time when the other one closes, it is advantageous to derive two square pulse sequences of the form shown in Fig. 5 from the carrier oscillation, in which the interpulse period is 240° and pulse width is 120° of a period, and the square pulse oscillations of both the switching four-poles are mutually shifted with respect to each other by 180°. Therewith it is ensured that only one of the two switching four-poles is switched on or

not short-circuited. With the aforementioned ratio of the pulse width to interpulse period, one has the advantage that the third harmonic of the switching frequency is not present in the generated pole-reversal function.

The switching four-pole networks SV1, SV2 according to Figures 2 and 3 are mutually exchangeable. There is also the possibility of substituting the field effect transistors FET 1 and FET 2 of the switching four-poles SV1 and SV2 according to Fig. 4 with commonly used transistors, which are to be connected with their emitter collector paths to the resistors R1 and R2 in series. Besides that, note that the switching four-poles with transistors connected in the series can also appear in place of the switching four-poles according to Figures 1 to 3.

5 Figures
8 Patent claims

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Patent Claims

1. Integrable active modulator or demodulator with single-ended input and single-ended output, characterized in that the modulator comprises an input stage with two separate outputs, giving the output signal with the same amplitudes, each of which is connected through a switching four-pole network at an output stage, that, further, the switching four-poles are in each case actuated alternately in cyclic timing of a carrier frequency oscillation, that, further, the output stage combines the output signals of the two switching four-pole networks, and that the phase of one of the two output signals of the input stage is shifted by 180° either in the input stage or after passing the corresponding switching four-pole network in the output stage

2. Modulator according to claim 1, in which the phase of one of the output signals in the input stage is shifted by 180° with respect to the phase of the other output signal, characterized in that the input stage is designed as a phase reversal stage with outputs which output two antiphase output signals with the same amplitude.

3. Modulator according to claim 1, in which the phase of one of the output signals of the input stage is shifted by 180° in the output stage, characterized in that the output stage is designed as a differential amplifier.

4. Modulator according to claim 1, characterized in that for the actuation of both the switching four-poles, two square pulse sequences with a mutual phase shift of 180°, derived from the carrier oscillation, are provided.

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5. Modulator according to claim 4, characterized in that the ratio of pulse width to interpulse period of the square pulse sequence derived from the carrier oscillation is selected to be less than 1, preferably less than 1/2.

6. Modulator according to one of the preceding claims, characterized in that in the switching four-pole field effect transistors are provided as switching elements.

7. Modulator according to one of the preceding claims, characterized in that the circuit comprises only resistors and semiconductor elements like transistors and diodes.

8. Modulator according to one of the preceding claims, characterized in that the modulator is foreseen especially for use in frequency converting digital filters.

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Fig.1

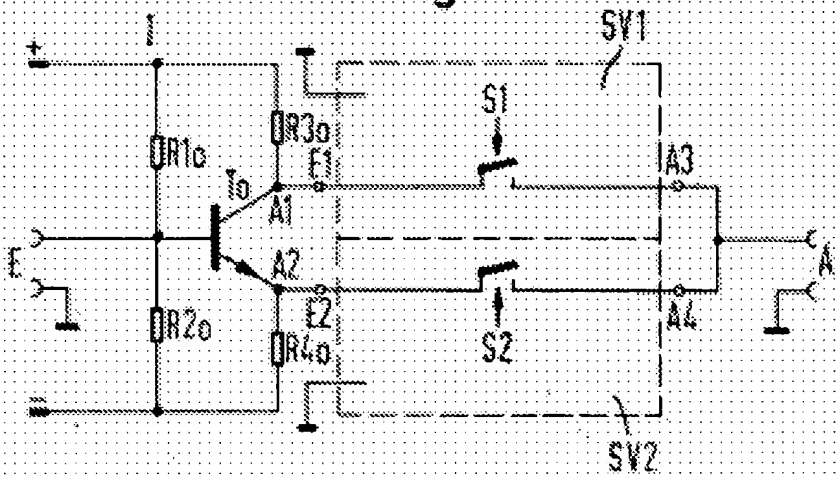

Fig.2

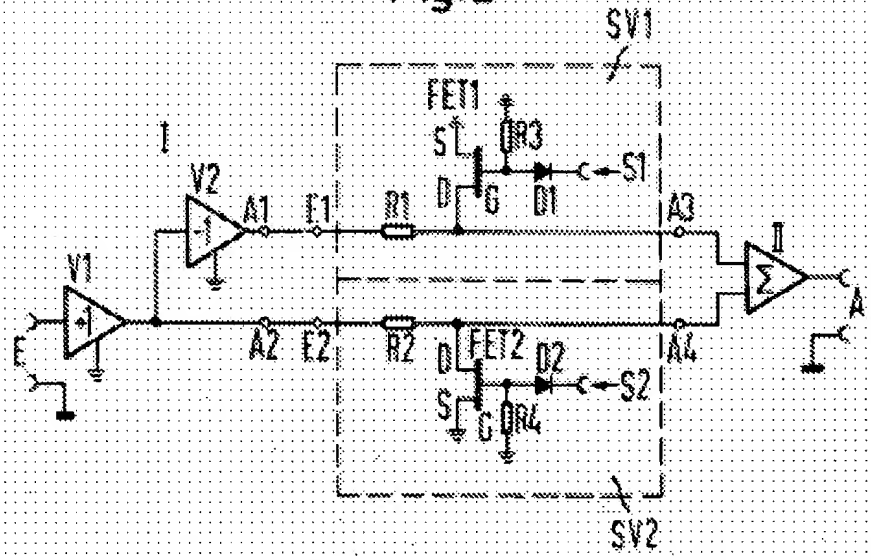

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Fig.3

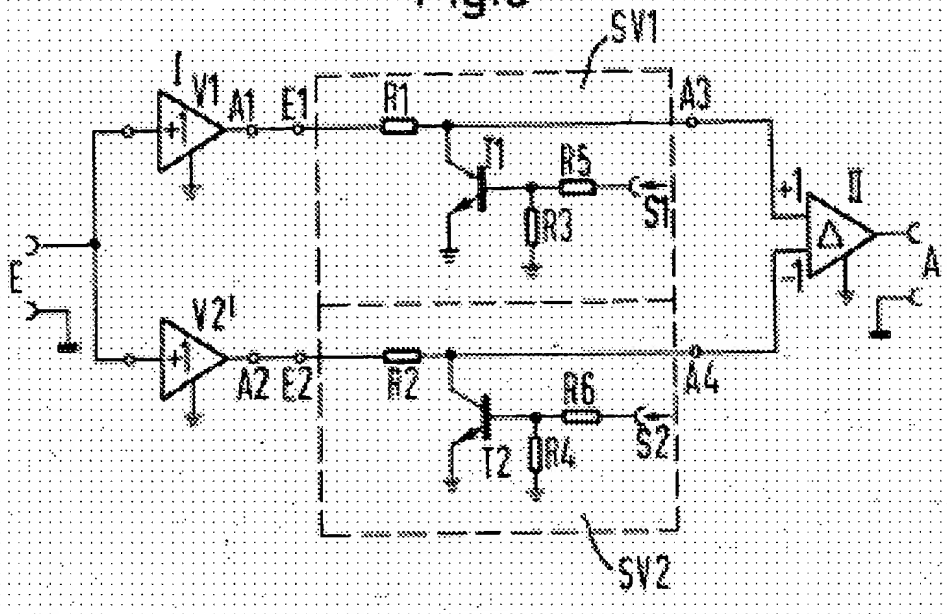

Fig.4

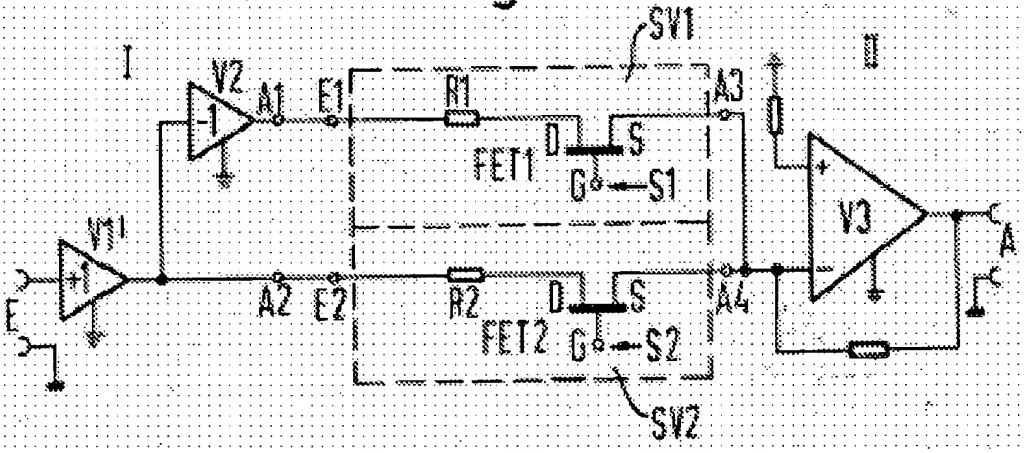
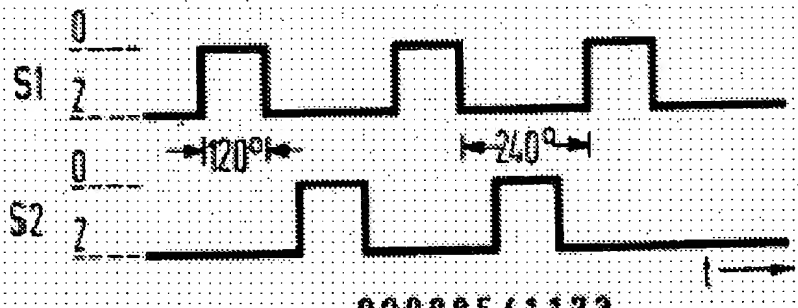
Fig.5